REMARKS

Claims 10, 11, 15, 16, 18 – 20 are pending. In the above-identified Office Action, the Examiner rejected Claims 10, 11, 15, 16, 18 – 20 under 35 U.S.C. § 102(b) as being anticipated by Bruce *et al.* (U.S. Patent No. 6,000,006) hereinafter 'Bruce'.

On receipt of the Office Action, Applicant's Attorney (William J. Benman) conducted a telephonic interview with the Examiner on May 9, 2007. During the interview, Mr. Benman and Examiner Flournoy discussed the Claims and the rejection thereof based on Bruce. No agreement was reached. However, the Examiner suggested that the appropriate course of action would be for Applicant to submit an Amendment After Final. Accordingly, the present paper is submitted as an Amendment After Final.

For the reasons set forth below, the present Application is believed to be in proper form for allowance. Reconsideration allowance and passage to issue are respectfully requested.

As stated previously, the present invention addresses the need in the art for a system or method for reducing average access times of slow memory technologies. In accordance with the invention, a system and method are taught for storing read and/or write pointer addresses in a buffer prior to power down. This data is used to provide for a rapid recovery on a reapplication of power so that processes may be resumed at the locations at which the processes were terminated. The inventive system discloses and claims a device with a processor programmed to cause a memory interface **to store memory addresses** that have been recently access **on the issuance of a power down command.**

The invention is set forth in Claims of varying scope of which Claim 15 is illustrative. Claim 15, as previously presented, recites:

> 15. A digital device that comprises:
> a memory having a **buffered memory interface** with one or more read buffers; and
> a processor coupled to the memory device and configured to retrieve stored information from the memory, **said processor being programmed to cause the memory to receive a power down command before electrical power is removed** from the memory **and the buffered memory interface to responsively store,** in a nonvolatile memory, **one or more addresses of memory locations that have been recently accessed.** (Emphasis added.)

None of the references teach, disclose or suggest the invention as presently claimed. That is, none of the references teach, disclose or suggest a device with a processor programmed to cause a memory interface **to store memory addresses** that have been recently access **on the issuance of a power down command.**

In the above-identified Office Action, the Examiner relied on Bruce in the rejection of the Claims. Bruce purports to show a system for wear-leveling non-volatile flash RAM mass storage. As to Claim 15, the Examiner suggested that at column 13, lines 31 – 34, Bruce teaches the storage of recently used addresses on receipt of a power down command. However, this assertion is not supported by the reference.

That is, at best, Bruce teaches a cache indexing or remapping scheme by which addresses are stored in a backup nonvolatile memory and used after an interruption of power. However, Bruce does not provide a teaching by which a processor issues a power down command and causes a buffer interface to **responsively** store recently used addresses in a nonvolatile memory.

As to Claim 10, note that Bruce does not teach a method including the steps of **detecting of a pending power down and storage,** in a nonvolatile memory, a read address for data buffered in a volatile read buffer.

In short, Bruce does not teach or suggest a system capable of detecting and responding to a pending power loss to enable a rapid recovery as set forth in Claims

10 and 15. Hence, Claims 10, 15, 20 and the Claims dependent thereon should be allowable.

Reconsideration, allowance and passage to issue are respectfully requested.

Respectfully submitted,
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